WHAT IS CLAIMED IS:

1. A fuse arrangement comprising:

a first fuse having a first end and a second end; and

a second fuse having a first end and a second end,

wherein the first end of the first fuse is spaced by a first interval from the first end of the second fuse, and the second end of the first fuse is spaced by a second interval from the second end of the second fuse, the second interval being different than the first interval; and wherein the first ends of the first and second fuses have widths narrower than or identical to those of the second ends of the first and second fuses.

2. The fuse arrangement according to claim 1, wherein the first interval is wider than the second interval and the first ends of the first and second fuses are disposed at a cutting region.

3. The fuse arrangement according to claim 1, wherein the first and second ends of the first and second fuses are disposed in a row direction.

4. The fuse arrangement according to claim 2, wherein the first and second ends of the first fuse are connected in a straight line and the first end of the second fuse is laterally offset from the second end of the second fuse.

5. The fuse arrangement according to claim 4, further comprises a third fuse and a fourth fuse, the first and second fuses forming a first fuse group and the third and fourth fuses forming a second fuse group,

wherein the second fuse group is positioned such that the second fuse group is adjacent to the first fuse group and the second fuse group is rotated one hundred eighty (180) degrees from the first fuse group.

6. The fuse arrangement according to claim 2, wherein the first ends of the first and second fuses are vertically connected to the second ends of the first and second fuses, respectively.

7. A fuse arrangement comprising:

a first fuse having a first end and a second end connected in a straight line;

a second fuse having a first end and a second end connected in a straight line;

a third fuse having a first end spaced by a first interval from the first end of the first fuse and a second end spaced by a second interval from the second end of the first fuse, the first end of the third fuse being laterally offset from the second end thereof; and

a fourth fuse having a first end spaced by the first interval from the first end of the second fuse and a second end spaced by the second interval from the second end of the second fuse, the first end of the fourth fuse being laterally offset from the second end thereof,

wherein the first ends of the first and third fuses have widths narrower than or identical to those of the second ends of the second and fourth fuses.

8. The fuse arrangement according to claim 7, wherein the first ends of the first to fourth fuses are disposed parallel in one row direction and the second ends of the first to fourth fuses are disposed parallel in another row

direction.

9. The fuse arrangement according to claim 7, wherein the first interval is wider than the second interval.

10. The fuse arrangement according to claim 7, wherein the first ends of the first and third fuses are disposed at a first cutting region formed along a first row and the second ends of the second and fourth fuses are disposed at a second cutting region formed along a second row.

11. A fuse arrangement comprising:

a first fuse group including a plurality of first fuses each having a first end and a second end, wherein the first ends of the first fuses are spaced from one another, the first and second ends of one of the first fuses are connected in a straight line, and the first ends of remaining ones of the first fuses become laterally offset from the second ends thereof; and

a second fuse group including a plurality of second fuses each having a first end and a second end, wherein the first ends of the second fuses are spaced by a first interval from one another, the second ends of the second fuses are spaced by a second interval from one another, the first and second ends of one of the second fuses are connected in a straight line, and the first ends of remaining ones of the second fuses become laterally offset from the second ends thereof,

wherein the first and second fuses having the first and second ends connected in a straight line are disposed to encompass the remaining of the first and second fuses; and wherein the first ends of the first and second fuses in the first and second fuse groups have widths narrower than or identical to

those of the second ends thereof.

12. The fuse arrangement according to claim 11, wherein the first ends of the first and second fuses are disposed parallel in one row direction and the second ends of the first and second fuses are disposed parallel in another row direction.

13. The fuse arrangement according to claim 11, wherein the first interval is wider than the second interval, the first ends of the first fuses are disposed at a first cutting region formed along a first row, and the second ends of the second fuses are disposed at a second cutting region formed along a second row.

14. A fuse arrangement comprising:

first fuse segments spaced by a first interval from each other;

second fuse segments each corresponding to the first fuse segments and disposed at a cutting region, the second fuse segments being spaced by a second interval from each other; and

a common connection line connected to the second fuse segments,

wherein the first fuse segments are orthogonally connected to second corresponding fuse segments respectively, the second interval is wider than the first interval, and a width of each of the second fuse segments is identical to or narrower than that of each of the first fuse segments.

15. The fuse arrangement according to claim 14, further comprising a fuse group having a third fuse segment and a fourth fuse segment and disposed adjacent to a fuse group of the first and second fuse segments so as to

have a symmetrical shape.

16. The fuse arrangement according to claim 15, wherein the third and fourth fuse segments are disposed to have the same structure as the first and second fuse segments.

17. The fuse arrangement according to claim 14, further comprising a fuse group which has a third fuse segment and a fourth fuse segment and is disposed adjacent to a fuse group of the first and second fuse segments and the common connection line so as to have a symmetrical shape.

18. The fuse arrangement according to claim 17, wherein the third and fourth fuse segments are disposed to have the same structure as the first and second fuse segments.

19. The fuse arrangement according to claim 14, wherein the first fuse segments are disposed parallel along a row direction and the second fuse segments are disposed parallel along a column direction.

20. A fuse arrangement comprising:

a first fuse and a second fuse that are disposed at a first fuse region and are spaced by a first interval from each other;

a first signal line and a second signal line that are connected to the first and second fuses, respectively, and are spaced by a second interval from each other;

a third fuse and a fourth fuse that are disposed at a second fuse region and are spaced by the first interval from each other; and

a third signal line and a fourth signal line that are connected to the third and fourth fuses, respectively, and are spaced by the second interval from each other,

wherein the first and second signal lines are disposed adjacent to the second fuse region, the third and fourth signal lines are disposed adjacent to the first fuse region, and the first interval is wider than the second interval.

21. The fuse arrangement according to claim 20, wherein the first signal line is connected to one end of the first fuse in a straight line and the second signal line is connected to the second fuse so as to be laterally offset by a predetermined angle from one end of the second fuse.

22. A semiconductor memory device comprising:

an array of memory cells arranged in rows and columns;

a redundant array for replacing defective memory cells; and

a plurality of fuse boxes for storing defect addresses, respectively,

wherein each fuse box includes a first fuse having a first end and a second end connected in a straight line and a second fuse having a first end spaced by a first interval from the first end of the first fuse and a second end spaced by a second interval from the second end of the first fuse; and

wherein the first ends of the first and second fuses are disposed at a cutting region along a row direction, the first end of the second fuse is laterally offset from the second end of the second fuse, and the first ends of the first and second fuses have widths identical to or narrower than those of the first and second fuses.

23. The semiconductor memory device according to claim 22,

wherein each fuse box further comprises a second fuse group having third and fourth fuses, the second fuse group is positioned such that a first fuse group of the first and second fuses is adjacent to the second fuse group and the second fuse group is rotated one hundred eighty (180) degrees from the first fuse group.

24. The semiconductor memory device according to claim 23, wherein the third and fourth fuses are disposed to have the same structure as the first and second fuses.

25. A semiconductor memory device comprising:

a plurality of word lines arranged in parallel in a row direction;

a plurality of bit lines arranged in parallel in a column direction;

a plurality of memory cells connected to the word lines and the bit lines;

a plurality of fuse boxes for storing defective address information;

a row select circuit for selecting one of the word lines in response to decoded signals;

first signal lines connected to the row select circuit and the fuse boxes and disposed at one side of the fuse boxes;

second signal lines connected to the row select circuit and disposed at the one side of the fuse boxes; and

third signal lines connected to the fuse boxes and disposed at the other side of the fuse boxes.

26. The semiconductor memory device according to claim 25, wherein the second and third signal lines transfer the same signals.

27. The semiconductor memory device according to claim 25, wherein loading of the second and third signal lines is more than that of the first signal lines.

28. The semiconductor memory device according to claim 25, wherein the plurality of fuse boxes include a first fuse box group disposed in a row direction and a second fuse box group positioned such that the second fuse box group is disposed adjacent to the first fuse box group and the second fuse box group is rotated one hundred (180) degrees from the first fuse box group.

29. The semiconductor memory device according to claim 28, wherein the first signal lines are connected to the first fuse box group and the third signal lines are connected to the second fuse box group.

30. The semiconductor memory device according to claim 29, wherein the third signal lines are the same as the second signals.